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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,730	12/01/2003	Mauricio J. Serrano	42P17023	3094

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EXAMINER	
DUDEK JR, EDWARD J	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,730	SERRANO ET AL.	
	Examiner	Art Unit	
	Edward J. Dudek	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the application filed on 01 December 2003.

Claims 1-30 have been presented for examination.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: figure 4, elements 425 and 440. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites the limitation "the processing monitoring hardware" in line 6. There is insufficient antecedent basis for this limitation in the claim. For the remainder of this Office Action this limitation will be construed as the performance monitoring hardware.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 8, 11-12, 19, 22, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Eberhard (U.S. Patent Application Publication #2002/0078264).

Referring to claim 1: Eberhard teaches a processor comprising: an execution unit (see [0019]); and a buffer to store data regarding each of a plurality of loads executed by the processor (see [0018], lines 10-11).

Referring to claim 2: the buffer is a part of performance monitoring hardware to monitor processor operations (see [0018], lines 7-11).

Referring to claim 8: further comprising a filter, the filter determining whether the execution of each of the plurality of memory operations meets a criterion for storage (see [0033]).

Referring to claim 11: Eberhard teaches a method comprising: monitoring the execution of a plurality of memory operations by a processor (see [0021]); and storing information in a buffer regarding the execution of the plurality of memory operations (see [0018], lines 7-11).

Referring to claim 12: the buffer is implemented in hardware (see [0019]).

Referring to claim 19: filtering each of the plurality of memory operations to determine whether to store information regarding the execution of the operation in the buffer (see [0033]).

Referring to claim 22: Eberhard teaches a system comprising: a bus (see figure 1, element 118); a processor coupled to the bus (see figure 1, element 102), the processor comprising: an execution unit (see [0019]); performance monitoring hardware to monitor operations of the execution unit (see [0018], lines 7-11), the processing monitoring hardware including a buffer to store data regarding each of a plurality of loads executed by the processor (see [0018], lines 10-11); and a cache memory (see [0019]).

Referring to claim 28: further comprising a filter, the filter determining whether the execution of each of the plurality of loads meets a criterion for storage (see [0033]).

Claims 1-3, 5-7, 9-12, 15-18, and 20-21 are rejected under 35 U.S.C. 102(e/a) as being anticipated by Talcott et al (U.S. Patent Application Publication #2003/0188226).

Referring to claim 1: Talcott teaches a processor comprising: an execution unit (see [0017]); and a buffer to store data regarding each of a plurality of loads executed by the processor (see [0018]).

Referring to claim 2: the buffer is a part of performance monitoring hardware to monitor processor operations (see [0018]).

Referring to claim 3: the software is to determine relationships between the executed loads based on the stored data (see [0021], lines 8-10).

Referring to claim 5: the buffer comprises a circular buffer (see [0021]).

Referring to claim 6: the data stored for each of the plurality of memory operations includes an instruction address (see claim 7).

Referring to claim 7: the data stored for each of the plurality of memory operations includes an effective address (see claim 7).

Referring to claim 9: the buffer is to be frozen upon the occurrence of a condition (see [0021], lines 8-10, and [0023]).

Referring to claim 10: the condition comprises a miss in a cache, a memory exception, or a programmed event that matches a criterion (see [0021], lines 6-10).

Referring to claim 11: Talcott teaches a method comprising: monitoring the execution of a plurality of memory operations by a processor (see [0017] and [0018]);

and storing information in a buffer regarding the execution of the plurality of memory operations (see [0018]).

Referring to claim 12: wherein the buffer is implemented in hardware (see [0018]).

Referring to claim 15: the stored information includes an instruction address for each of the plurality of memory operations (see claim 7).

Referring to claim 16: the stored information includes an effective address for each of the plurality of memory operations (see claim 7).

Referring to claim 17: determining the base address of a memory operation based on the stored information (see claim 7).

Referring to claim 18: further comprising deleting the oldest information in the buffer when new information regarding the execution of a load is stored (see [0021] and [0024]).

Referring to claim 20: further comprising halting the storing of information when a condition is met (see [0021], and [0023]).

Referring to claim 21: wherein the condition comprises a cache memory miss, a memory exception, or a programmed event that matches a criterion (see [0021]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-23, 25-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talcott et al (U.S Patent Application Publication #2003/0188226) in view of Brock et al (U.S. Patent #6,601,149).

Referring to claim 22: Talcott teaches a system comprising: a bus; a processor (see [0017]), the processor comprising: an execution unit (see [0017]); performance monitoring hardware to monitor operations of the execution unit (see [0018]), the processing monitoring hardware including a buffer to store data regarding each of a plurality of loads executed by the processor; and a cache memory (see [0018]). Talcott does not teach the processor being coupled to a bus. Systems comprising a processor coupled to a bus are well known in the art, and are illustrated by Ravichandran (see figure 1). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have coupled the processor, taught by Talcott, to a bus to create the system illustrated by Ravichandran since this architecture is well known and commonly used.

Referring to claim 23: Talcott teaches wherein software is allowed to access the data stored in the buffer (see [0021], lines 8-10).

Referring to claim 25: the buffer comprises a circular buffer (see [0021]).

Referring to claim 26: Talcott teaches the data stored regarding each of the plurality of loads includes an instruction address (see claim 7).

Referring to claim 27: Talcott teaches the data stored regarding each of the plurality of loads includes an effective address (see claim 7).

Referring to claim 29: Talcott teaches the operation of the buffer is halted upon the occurrence of a condition (see [0021] and [0023]).

Referring to claim 30: Talcott teaches the condition comprises a miss in the cache memory, a memory exception, or a programmed event that matches a criterion (see [0021]).

Claims 4, 13-14, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talcott et al (U.S. Patent Application Publication #2003/0188226) in view of Brock et al (U.S. Patent #6,601,149).

Referring to claim 4: Talcott teaches all the limitations of claims 1-3 as discussed above, however, Talcott does not teach using the software to determine relationships between the executed loads and the stored data. Brock teaches a performance monitoring system that allows the user to see a graphical representation of the data, and allows the user to select various ways to visualize the data (see column 7, lines 40-61). This allows the user to discover any performance abnormalities or inefficiencies with the memory system (see column 7, lines 50-55). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system taught by Talcott, to allow the software to determine relationships on the stored data, as taught by Brock, to allow the user to discover any performance abnormalities or inefficiencies with the memory system.

Referring to claims 13 and 14: Talcott teaches all the limitations of claim 11 as discussed above, however, Talcott does not teach using the software to determine

relationships between the executed loads and the stored data. Brock teaches a performance monitoring system that allows the user to see a graphical representation of the data, and allows the user to select various ways to visualize the data (see column 7, lines 40-61). This allows the user to discover any performance abnormalities or inefficiencies with the memory system (see column 7, lines 50-55). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system taught by Talcott, to allow the software to determine relationships on the stored data, as taught by Brock, to allow the user to discover any performance abnormalities or inefficiencies with the memory system.

Referring to claim 24: Talcott teaches all the limitations of claims 22-23 as discussed above, however, Talcott does not teach using the software to determine relationships between the executed loads and the stored data. Brock teaches a performance monitoring system that allows the user to see a graphical representation of the data, and allows the user to select various ways to visualize the data (see column 7, lines 40-61). This allows the user to discover any performance abnormalities or inefficiencies with the memory system (see column 7, lines 50-55). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system taught by Talcott, to allow the software to determine relationships on the stored data, as taught by Brock, to allow the user to discover any performance abnormalities or inefficiencies with the memory system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent #6,772,322: teaches storing tags that hold performance data for an instruction.

U.S. Patent #6,748,558: teaches a real time performance monitor built into a processor that monitors memory accesses.

U.S. Patent #6,748,522: teaches sampling instructions issued from a process to track their performance.

U.S. Patent Application Publication #2005/0071822: teaches tracking memory accesses to certain ranges of memory for performance evaluation or programs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward J. Dudek whose telephone number is 571-270-1030. The examiner can normally be reached on Mon thru Thur 7:30-5:00pm Sec. Fri 7:30-4 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Edward Dudek
December 5, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
12/07/06